PROCESS OF FORMING METAL SURFACES COMPATIBLE WITH A WIRE BONDING AND SEMICONDUCTOR INTEGRATED CIRCUITS MANUFACTURED BY THE PROCESS

Cross-Reference to Related Applications

This application claims the benefit of U.S. provisional patent application no. 60/269500, filed on 16 February 2001, under § 119 (e).

Background of the Invention

Field of the Invention

The invention relates to a process of manufacturing a semiconductor integrated circuit and, in particular, a process of forming an electrical connection between a metal wire and a metal interconnect in the semiconductor circuit.

Description of the Related Technology

Wire bonding has been the predominate structure for connecting to a semiconductor interconnects and it is used in a significant share of all leaded packages. Briefly, a wire bonding is a low-temperature welding process. As an alternative technique to welding, conventional wire bonding uses ultrasonic energy that is applied through a bonding tool (called a capillary or wedge) to a wire and a bond site. This energy increases the dislocation density of the wire and bond site, lowering flow stress and modulus of elasticity while increasing the rate of diffusion. This causes the material to deform easily at much lower stresses than would otherwise be required.

Presently, with the development of copper chip technology by various semiconductor companies, the fabrication of microprocessors, digital signal processors, memories, and other semiconductor circuits will be made by using advanced copper interconnects. With INTEL's launch of the PENTIUM II microprocessor, which is code named Copper Mine, other manufacturers, such as AMD and MOTOROLA, have launched their own processors based on copper metal. This has brought about new

challenges in the packaging of a copper chip using conventional wire bonding technology. With conventional wire bonding technology, when the copper chip is mounted on the carrier substrate using a die bonding process generally cured at a temperature of 125 °C and a subsequent wire bonding process is performed at 110 - 180 °C, it causes oxidation of the copper metallization and forms improper ball bonding. The conventional gold/aluminum wire bonding in such a case has a very low bond strength. Another approach is to use a wire bonding with a reduction atmosphere by purging the bond with N_2/H_2 gas, but such an approach is more complex and not cost effective.

As one example of known wire bonding technology, an advanced copper interconnect system (U.S. Patent No. 5,785,236 entitled "Advanced Copper Interconnect System Compatible With Existing Bonding Technology") is illustrated in Figure 1. A gold wire bonding (gold wire not shown) is carried out by applying an aluminum pad 13 over a copper interconnects 12 and a dielectric 11. These are deposited on a silicon wafer 10, through an opening formed on a passivation layer 14. As shown in Figure 1, this additional cap metallization (aluminum pad 13) process enables electrical connections to be formed between the gold wire (not shown) and the copper interconnects 12 through the aluminum pad 13. The system enables the conventional wire bonding techniques to be employed on the copper interconnects 12. However, the additional step of forming the aluminum pad 13 involves a complicated semiconductor fabrication process such as a lithography step and a chemical etching step, which increases manufacturing cost.

Another known bonding technique is depicted in Figure 2 (U.S. Patent No. 6,020,048 entitled "Thick film circuit board and method of forming wire bonding electrode thereon"). A copper thick film 21 (Cu conductor) is screen printed as a wiring layer on a ceramic substrate 20. Then, a thick gold film paste 22 (Au conductor) is screen printed at bonding locations on the substrate 20 such that at least a part of the thick gold film paste 22 is overlapped with the Cu conductor 21. Thereafter, a silicon chip 23 is bonded to the ceramic substrate 20 by an adhesive agent or die bond 24, and

the silicon chip 23 is bonded to the thick gold film paste 22 by a Au or Al wire 25. The structure shown in Figure 2 permits a gold/aluminum bonding by using conventional wire bonding. However, this method is applicable to only the copper metallization in the substrate 20, while the silicon chip 23 has conventional aluminum or gold wire compatible metallization. Secondly, it needs a mask and an additional screen printing process, aside from the fact that printing of gold material is not a cost-effective process.

Another known bonding technique is disclosed in U.S. Patent No. 6,034,422 and Singapore Patent SG60018A1 (entitled "Lead Frame, method for partial noble plating of said lead frame and semiconductor device having said lead frame"). Referring to Figure 3, a silver layer 32 is provided on a copper lead frame 31. A silicon chip 33 is bonded to a die pad 36 by an adhesive agent 34 (die bond) and the silicon chip 33 is bonded to the silver layer 32 by a wire 35 (wire bond). The silver layer 32 prevents oxidation of the copper lead frame 31 by providing a thin silver plating on the copper lead frame 31. This silver layer 32 will enhance the molding of the devices. However, this process is restricted to the copper lead frame area and the semiconductor device is considered to have a compatible metallization to the conventional Au and Al bonding wire.

Summary of Certain Inventive Aspects

One aspect of the present invention is to provide a process of forming metal surfaces on a bare metal chip. The metal chip includes metal interconnects formed on a semiconductor substrate and at least a portion of the metal interconnects is exposed to the environment. The process comprises applying a noble metal on the portion of the exposed metal interconnect and performing a chemical process that causes a layer of the noble metal to convert to a bondable layer compatible with a wire bonding. The process also comprises bonding a metal wire to the bondable layer.

Another aspect of the present invention is to provide a process of forming metal surfaces on a bare metal chip. The metal chip includes a metal interconnect formed on a semiconductor substrate and at least a portion of the metal interconnect is exposed to the environment. The process comprises depositing a layer of a low melting point metal whose melting temperature is relatively low on the portion of the exposed metal

interconnect. The process also includes performing a chemical process that causes the layer of the low melting point metal to convert into a bondable layer compatible with a wire bonding. The process also comprises bonding a metal wire to the bondable layer.

Another aspect of the present invention is to provide a process of forming metal surfaces on a bare metal chip. The metal chip includes a metal interconnect formed on a semiconductor substrate and at least a portion of the metal interconnect is exposed to the environment. The process further comprises depositing a layer of solder particles of a low melting point metal whose temperature is relatively low on the portion of exposed metal interconnect. The process also comprises converting the layer of the solder particles to a bondable layer compatible with a wire bonding, and bonding a metal wire to the bondable layer.

Still another aspect of the present invention is to provide a process of forming metal surfaces on a bare metal chip. The metal chip includes a metal interconnect formed on a semiconductor substrate and at least a portion of the metal interconnect is exposed to the environment. The process further comprises depositing a layer of solder particles of a noble metal or an alloy thereof on the portion of exposed metal interconnect. The process also comprises converting the layer of the solder particles to a bondable layer compatible with a wire bonding, and bonding a metal wire to the bondable layer.

Brief Description of the Drawings

Figure 1 is a schematic view of a conventional wire bonding system.

Figure 2 is a schematic view of another conventional wire bonding system.

Figure 3 is a schematic view of still another conventional wire bonding system.

Figure 4a is a schematic view of a manufactured copper chip.

Figure 4b is a schematic view as shown in Figure 4a, but adding a bondable layer to the copper interconnect according to the present invention.

Figure 5 is a schematic view of one embodiment according to the invention.

Figures 6a and 6b are schematic views of another embodiment according to the invention.

Figures 7a and 7b are schematic views of another embodiment according to the invention.

Figures 8a and 8b are schematic views of still another embodiment according to the invention.

Figure 9 is a schematic view of a semiconductor circuit in which the embodiment of the invention can be implemented.

Figure 10a is a schematic view of a manufactured copper chip.

Figures 10b and 11 are schematic views for comparing a conventional wire bonding system and the wire bonding system according to the invention.

Detailed Description of the Certain Inventive Embodiments

This invention relates to a process of forming metal surfaces in a semiconductor device with metal interconnects such as copper (Cu) interconnects, copper alloy, other possible combination of copper alloys, and other metal interconnects, using conventional Au and Al wire bond tools. The invention may be applied to metallization which is incompatible with conventional wire bonding. By using a suitable low cost intermediate process, according to this invention, a bond pad, which is a part of the Cu interconnect and exposed to the environment, is converted to a bondable layer that can be bonded to a conventional metal wire, such as an Au or Al wire (not shown).

Referring to Figure 4a, a bare Cu chip with the Cu interconnects 42 (Cu metallization layer) and a passivation layer 45 is shown. The Cu metallization layer 42 can be a single layer or multiple layers and it may also have a suitable barrier and adhesion layers using the conventional copper chip technology or dual damascene process. Reference numerals 41 and 44 refer to a dielectric layer.

Since the present invention is applied to the manufactured chip illustrated in Figure 4a, no additional process such as masking or etching is required at the front end (chip manufacturing process). A very simple low cost and maskless additional step at the assembly back end (chip packaging process) will convert a bond pad 43 (exposed copper interconnects) into a bondable surface with a bondable layer 46 as shown in

Figure 4b. After the bondable layer 46 is formed, a metal wire (not shown) such as an Au or Al may be bonded to the bondable layer 46 through a conventional wire bonding technique, for example, an ultrasonic wire bonding, a thermosonic wire bonding, a welding or a combination thereof.

The additional process steps may comprise one of the following modes described below:

MODE 1:

Referring to Figure 5, a noble metal (e.g., silver-Ag, gold-Au, platinum-Pt, palladium-Pd, an alloy thereof, etc.) is applied to the bond pad 43 (exposed Cu interconnects), and the bond pad 43 is replaced with a noble metal layer 51 which is a bondable layer compatible with a wire bonding. Here, a simple chemical process such as an immersion silver process, a dip silver process, an electroless silver process, etc., is used to deposit the noble metal layer 51 on the bond pad 43.

Specifically, when the noble metal is applied to the exposed Cu interconnects 43 by the above chemical process, a diffusion occurs on the exposed Cu interconnects 43, which causes Cu atoms of the exposed Cu interconnects 43 and atoms of the noble metal to mix with one another and, thus, the noble metal adheres to the exposed Cu interconnects 43. An immersion silver process is disclosed by others in the following patent documents. U.S. Patent Nos. 5,733,599 and 5,935,640, which are incorporated by reference. As described in the patents, the process results in an exchange of atoms between the copper and silver resulting in a layer of silver deposit on the Cu metallization.

After the noble metal is adhered to the exposed Cu interconnects 43, conventional wire bonding is carried out on the metalization, and the quality of the wire bond can be evaluated by shear strength. In one of the embodiments, the value of the shear strength falls within the JEDEC qualifying limits. (JEDEC stands for "Joint Electron Device Engineering Council", and is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronic industry.) This has been proven by experimentation and the results thereof which are incorporated as Appendix A of this application.

The chemical process may comprise any other processes that satisfy the above results. Also, the noble metal may comprise one or more of the other metals shown in Appendix B, besides Ag, Au, Pt and Pd.

As described above, the process is carried out on a bare semiconductor chip that has already been manufactured, and the process affects only the exposed copper interconnects 43, and hence no mask is required. The noble metal is restricted to adhere only to the Cu interconnects 42, even if masks are not used, because an exchange reaction of atoms does not occur on the passivation layer 45. Even if most of the back end houses are generally not equipped with photolithographic equipment and masks, the process of the invention is very conveniently performed at either a front end or a back end. After this process is completed, the bonding between gold or aluminum wires (not shown) and the noble metal layer can be easily carried out through the conventional way, such as ultrasonic wire bonding, thermosonic wire bonding, a welding or combination thereof, etc.

MODE 2:

Referring to Figure 6a, a low melting point metal is applied to the exposed Cu interconnects 43. The low melting point metal means solder materials whose temperature is relatively low (below 350°C) suitable for soldering purpose. By way of example, the low melting point metal may comprise Tin (Sn), Indium (In), Bismuth (Bi), Lead (Pb), and an alloy thereof, etc. A simple chemical process such as electroless tin, dip tin, electroless bismuth, etc. is used to replace a few mono layers of the exposed Cu interconnects 43 with a thin layer of the low melting point metal 61. The electroless tin process is disclosed in U.S. patent No. 3,917,486 and 4,027,055, which are incorporated herein by reference. The simple chemical process also comprises any other processes that satisfy the above results in addition to the electroless tin, dip tin, and electroless bismuth, etc.

After depositing the layer of the low melting point metal 61 over the bond pad 43, a chemical reaction such as sintering and metal replacement, a heat treatment (reflow process, soldering), or combination thereof may be additionally carried out to

increase the adhesion of the deposited low melting point metal. The above process including the heat treatment, etc., ensures that the fine solder particles of the low melting point metal are melted and form a thin coat of material over the exposed copper interconnects 43. The heat treatment may convert partially or fully the thin layer of the low melting point metal into an intermetallic bondable layer 62 compatible with a conventional wire bonding. For example, by cooling tin and reflowing it over copper, Cu_6Sn_5, which constitutes the intermetallic bondable layer 62, is formed, However, not all of the low melting point metals need the heat treatment step to form the bondable layer 62. A thin layer of a metal such as In or Bi may form a bondable layer without use of heat treatment. The bondable layer 62 is used for bonding a metal wire with conventional wire bonding. However, the layer 61 of metal, such as In or Bi, which is applied after the simple chemical process, can be directly used for wire bonding without any heat treatment being performed.

The process in MODE 2 is also carried out on a bare semiconductor chip that has already been manufactured as illustrated in Figures 6a and 6b, and the process affects only the exposed copper interconnects 42, and hence no mask is required. After this process is done, the bonding between gold or aluminum wires (not shown) and the bondable layer 62 can also be easily carried out in the conventional way, such as ultrasonic wire bonding, thermosonic wire bonding, welding or combination thereof, etc.

MODE 3:

As shown in Figure 7a, a tacky (sticky) layer 71 is provided on the exposed copper interconnects 43 by known chemical processes. Solder particles formed from low melting point metal are deposited on the tacky layer 71. The solder particles are embedded into the tacky layer 71, thus a layer of the solder particles is formed on the exposed copper interconnects 43. Since the solder particles have been embedded into the tacky layer 71, the layer of the solder particles will also be designated as reference numeral 71 in Figure 7a.

After the layer 71 is deposited on the bond pad 43, a chemical reaction, a heat treatment (reflow process, soldering), or combination thereof may be additionally carried out to increase the adhesion of the deposited layer of the solder particles. A bondable layer 72 which has undergone the above process (heat treatment, chemical reaction, etc.) is shown in Figure 7b. The bondable layer 72 is used for bonding a metal wire with conventional wire bonding. However, the layer 71 can be directly used for wire bonding before the heat treatment is performed.

The above processes may be performed by using SUPER JUFFIT process of Showa Denko (http://www.sdk.co.jp) or SUPER SOLDER process of Harima Chemical Inc. (http://www.harima.co.jp).

The process described in MODE 3 is also a simple chemical process which can be carried out directly on the exposed copper interconnects 43 without any masks.

MODE 4:

As shown in Figure 8a, a tacky (sticky) layer 81 is provided on the exposed copper interconnects 43 by known chemical processes. Fine particles of a noble metal or its alloy are deposited on the tacky layer 81. The fine particles are embedded into the tacky layer 81, thus a layer of the fine particles of a noble metal or its alloy is formed on the exposed copper interconnects 43. Since the fine particles have been embedded into the tacky layer 81, the layer of the fine particles will also be designated as reference numeral 81 in Figure 8a.

After the layer 81 is deposited on the bond pad 43, a chemical reaction, a heat treatment (reflow process, soldering), or combination thereof is carried out in order to form a bondable layer 82 compatible with conventional wire bonding as shown in Figure 8b. The layer 81 may comprise fine particles of any noble metals or their combination which can be reduced and sintered into a bondable metal layer by a heat treatment or a chemical reaction. The bondable layer 82 is used for bonding a metal wire with conventional wire bonding.

The above processes may be performed by using SUPER JUFFIT process of M/s Showa Denko (http://www.sdk.co.jp) or SUPER SOLDER process of M/sHarima Chemical Inc. (http://www.harima.co.jp).

The process described in MODE 4 is also a simple chemical process which can be carried out directly on the exposed copper interconnects 43 without any masks.

MODES 1 and 4 may be further described.

A wire bonding or a bare Cu chip is a back end or assembly house issue. In the prior art, the process could only be carried out in a semiconductor chip fabrication house, which uses a costlier sputtering and etching tool. The prior art involves sputtering an aluminum layer on copper, and then carrying out the passivation and sending it to assembly houses for wire bonding. However, in the present invention the same process is carried out on a bare Cu chip which has already been sent to the assembly house. It is a simple chemical process which converts the exposed copper layer into a bondable layer, thus permitting a wire bonding using conventional Au and Al wire bonders.

Furthermore, the process according to the invention can also be additionally applied to any structure formed on the semiconductor substrate on which the wire bonding is carried out. The structure includes any shape or form (e.g. thick, thin, round, square, with via, etc.) that a bond pad tae. Also, it is not strictly restricted to conventional bond pads alone. In addition, the structure includes any device surface on which the process provided by the process of the invention is applied.

MODE 5:

As illustrated in Figure 9, the above processes and methods described in MODE 1 to MODE 4 can also be implemented on multilayer advanced copper interconnects with a low K dielectric 91 and a passivation layer 93. The low K dielectric 91 may be, by way of example, comprises SiLK®, Black Diamond®, and Coral®. Also, the range of the low K dielectric 91 may be between 0-3. Reference numeral 92 in Figure 9 indicates a Cu interconnects.

Figures 10a-11 are drawings for comparing the prior art and the present invention. Figure 10a illustrates a conventional bare Cu chip. Figure 10b illustrates one of the prior wire bonding techniques that use Al cap metallization. Figure 11 illustrates a wire bonding technique according to the present invention.

Figure 10a is substantially the same as Figure 4a. A silicon wafer 100 and an oxide/dielectric layer 102 in Figure 10a corresponds to a silicon layer 40 and a dielectric 41 in Figure 4a. A Cu metallization 101 in Figure 10a corresponds to the Cu interconnects 42 shown in Figure 4a.

Figure 10b is substantially the same as Figure 1. An Al cap metallization 104 in Figure 10b corresponds to an Al pad 13 in Figure 1. As described before, forming the Al cap metallization on the Cu metallization involves a complicated process such as lithography and chemical etching, resulting in a high manufacturing cost.

Figure 11 illustrates one embodiment of the present invention. A bondable layer 111 formed by the process of the present invention is compatible with conventional wire bonding technique, such as an ultrasonic wire bonding, a thermosonic wire bonding, a welding or combination thereof. The main diffenrece between the process of Figure 11 and the process of Figure 10b is that the process of Figure 11 uses a simple chemical process to form the bondable layer 111, while the process of Figure 10b uses a complicated semiconductor fabrication process to form the Al cap metallization 104.

RESULTS

Since the process of the present invention is performed on a processed chip, the present invention has passivation followed by the metallization layer being converted into a bondable layer by the process described in Modes 1-5.

The results of the wire bonding experiments carried out is documented in Appendix A. Page 1/7 of Appendix-A illustrates wire bond process parameters. Page 2/7 of Appendix-A illustrates Pull-strength test results. Page 3/7 of Appendix-A illustrates photographs showing Failure mode of page 2/7 test. Page 4/7 of Appendix-A illustrates Pull-strength test results under 1 time and 4 times reflowing in an oven of 0-260°C (5mins) Page 5/7 of Appendix-A illustrates photographs showing Failure mode of page 4/7 test. Page 6/7 of Appendix-A illustrates shear strength test results under (1) time zero and (2) Thermal Cycle -40°C - 125°C, 15min, interval for 94 cycles. Page 7/7 of Appendix-A illustrates Pull-strength test results under 150°C for 1 hour, before gold

ball bonding and 240 hours, before wedge bonding respectively. All the data of Appendix-A are based on MODE 1.

In summary, the values of wire bond pull strength and shear strength by the wire bonding of the invention are equivalent to the values achieved by conventional wire bonding. Also, referring to page 2/7 of Appendix-A, it can be seen that no degradation has occurred. Page 2/7 of Appendix-A shows Pull strength tests under (1) Time Zero; (2) HTS-High Temperature Storage (150°C for 240 hours); and (3) Thermal Cycle: -40°C - 125°C, 15 mins. for 94 cycles. Comparison of the average pull strength results, (1) 9.515, (2) 9.015 and (3) 9.568 on page 2/7 of Appendix-A shows no substantial degradation. Hence, this technique can be widely applied to carry out conventional wire bonding on Cu-chips.

CERTAIN ADVANTAGES OF THE INVENTION

The present invention is so simple, it can be easily applied to finished semiconductor devices with Cu metallization. It generally does not require any additional processes in the front end.

The present process is so flexible that it can be easily incorporated either at front-end or in the backend assembly

The present process is a simple method which can be carried out directly on the finished die. No additional masks are required for the fabrication and this reduces the cost drastically.

The other main advantage of this process is that it can be carried out at a die or wafer level. All other known prior art processes can only be carried out only on wafer level.

The process is suitable for both mass scale production as well as small-scale production.

The novelty of the process is such that it also allows the user to subject to all other temperature applied to the real package assembly process, which may cause oxidation of the copper metallization, such as die bonding process, reflow component attach process, etc.

Lastly, this inventive process is not labor intensive.

Thus, there has been described a new wire bonding process and structure. While the preferred embodiment of the invention has been shown, apparently many changes and modifications may be made therein without departing from the scope of the invention. It is appreciated, therefore, that the appended claims cover any and all such changes and modifications which do not depart from the true spirit and scope of the invention.

Equipment : ESEC 3018
Material : Gul Tech BGA Substrate, Copper chip plated with silver, QMI581, 1.0mils gold wire.
Bonding sequence: Chip to lead frame lead
Equipment parameters:

Ball bond force	:	400mN
Ball bond time	:	20ms
Ball US Power	:	14.1%
Wedge bond force	:	700mN
Wedge bond time	:	20ms
Wedge US power	:	18.0%
Heater temperature	:	180 degree Celsius
Pre US ball power	:	0%
Ball US power	:	14.1%
Ball US power compensation	:	0.00
Ball US profile	:	Square
Ball delay force to US on	:	2.0ms
Pre US wedge power	:	0.0%
Wedge US power	:	18.0%
Wedge US power compensation:		0.40
Wedge US profile	:	Square
Wedge delay force to US on	:	2.0ms

Loop parameters:

Loop Mode	:	4:engineering
Loop factor A	:	0.960
Ball security height	:	0.200
Reverse length	:	0.150
Reverse height	:	0.200
Reverse length 2	:	0.150
Reverse height 2	:	0.150
Loop height	:	300um

EFO parameters:

Efo parameter select	:	auto
Wire diameter	:	25um
Free air ball diameter	:	60um

Note: wire length is around 4mm.

Sample 1/2/3 : Copper chip (plated with silver) mounted on BGA substrate using QMI518

Curing profile : 150 degrees Celsius for 1hr.

Bonding equipment: ESEC 3018 Wire Bonder

Time Zero		HTS (150 degrees for 240hr)		T/C (-40/125 deg C 15 mins Interval for 94 cycles)	
Pull strength (grams)	Failure Mode	Pull strength (grams)	Failure Mode	Pull strength (grams)	Failure Mode
9.502	1	7.962	1	8.889	1
10.254	1	9.007	1	9.105	1
10.382	1	8.486	1	9.734	1
9.575	1	8.948	1	9.314	1
10.050	1	8.574	1	9.104	1
9.485	1	9.109	1	9.391	1
9.935	1	10.015	1	9.522	1
9.676	1	9.749	1	9.07	1
10.00	1	9.673	1	9.799	1
9.771	1	9.961	1	10.027	1
9.833	1	9.027	1	8.668	1
9.647	1	8.727	1	9.756	1
9.613	1	8.624	1	10.182	1
9.796	1	9.341	1	9.953	1
9.743	1	9.325	1	9.641	1
9.429	1	9.880	1	9.178	1
10.183	1	9.425	1	9.812	1
9.619	1	9.496	1	9.362	1
10.105	1	8.477	1	9.958	1
9.349	1	8.707	1	9.908	1
8.252	1	8.702	1	9.035	1
9.079	1	8.901	1	9.833	1
8.990	1	8.773	1	9.032	1
9.648	1	8.808	1	9.339	1
9.479	1	8.658	1	9.445	1
9.447	1	9.845	1	10.048	1
9.444	1	8.799	1	9.835	1
8.723	1	8.470	1	10.336	1
8.718	1	8.805	1	9.791	1
9.229	1	8.592	1	9.96	1
8.847	1	8.011	1		
8.668	1	8.549	1		
Average = 9.515		Average = 9.015		Average = 9.568	

Failure Mode : 1 – break at neck (First Bond)

4 – break at heel (Second Bond)

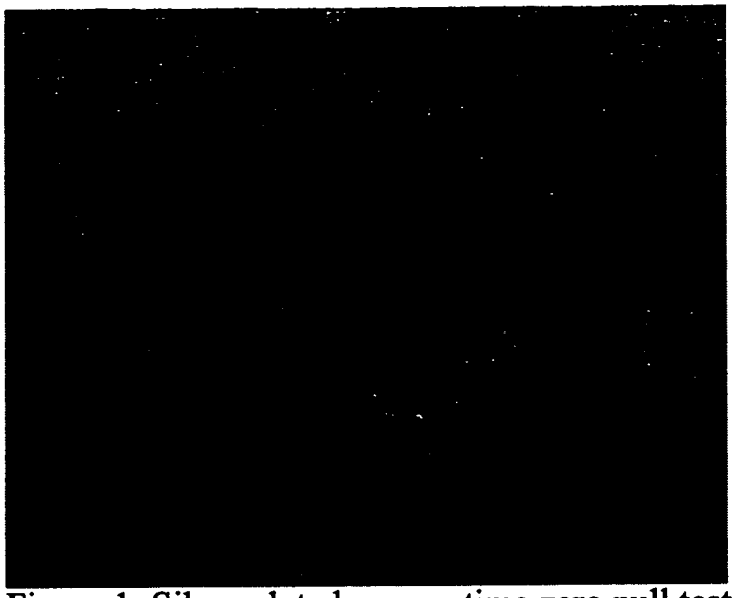

Figure 1: Silver plated copper time zero pull test - breaks at first ball bond.

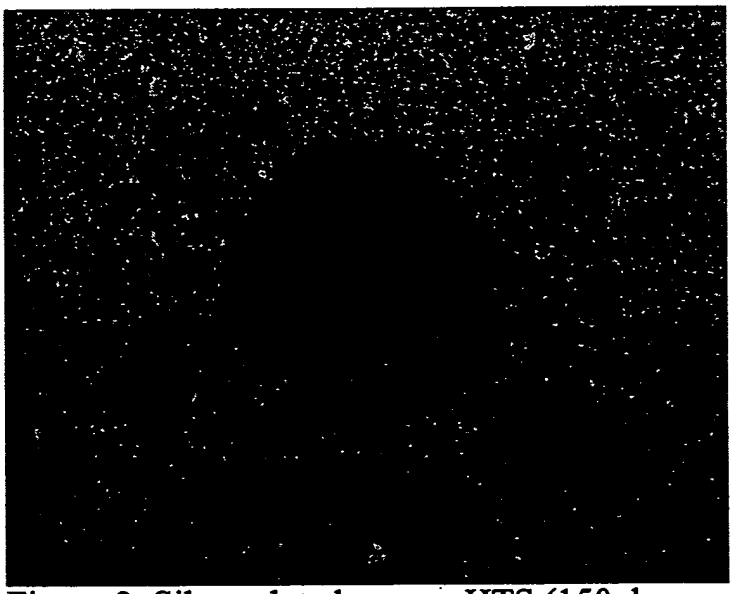

Figure 2: Silver plated copper HTS (150 degrees Celsius)240hr pull test - breaks at first ball bond.

Sample 4/5 : Copper chip (plated with silver) mounted on BGA substrate using QMI518

Curing profile : 150 degrees Celsius for 1hr.

Bonding equipment: ESEC 3018 Wire Bonder

1 x reflow		4x reflow	
Pull strength (grams)	Failure Mode	Pull strength (grams)	Failure Mode
9.257	1	9.112	1
9.298	1	9.338	1
9.139	1	8.910	1
9.721	1	9.007	1
9.037	1	8.897	1
8.641	1	9.100	1
9.245	1	9.118	1
9.818	1	9.434	1
9.390	1	9.164	1
9.195	1	9.708	1
9.773	1	8.742	1
9.795	1	9.249	1
9.697	1	8.597	1
9.725	1	9.026	1
9.290	1	9.164	1
8.984	1	9.448	1
9.346	1	8.109	1
9.583	1	9.031	1
9.456	1	9.396	1
9.704	1	9.163	1
8.265	1	8.474	1
9.003	1	8.950	1
8.843	1	8.950	1
9.029	1	9.375	1
9.144	1	8.729	1
9.075	1	8.836	1
9.312	1	8.222	1
9.349	1	9.181	1
9.679	1	9.361	1
9.653	1	8.973	1
9.087	1	9.298	1
9.385	1	9.158	1
Average = 9310		Average = 9.038	

Failure Mode: 1 – break at neck (First Bond)
4 – break at heel (Second Bond)

Figure 3: Silver plated copper 1xreflow pull test - breaks at first ball bond.

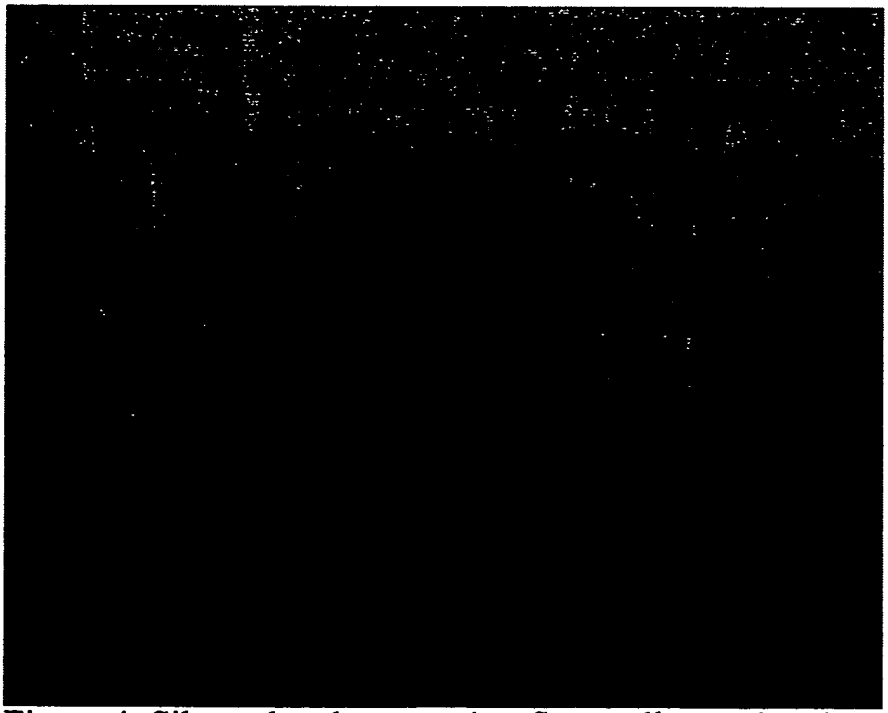

Figure 4: Silver plated copper 4xreflow pull test - breaks at first ball bond.

Sample 6/7 : Copper chip (plated with silver) mounted on BGA substrate using QMI518

Curing profile : 150 degrees Celsius for 1hr.

Bonding equipment: ESEC 3018 Wire Bonder

Time Zero		T/C (-40/125 deg C 15 mins Interval for 94 cycles)	
Ball Shear (grams)	Failure Mode	Ball Shear (grams)	Failure Mode
27.10	1	34.80	1
33.00	1	32.00	1
31.60	1	27.80	1
29.70	1	30.10	1
31.50	1	36.20	1
35.50	1	30.10	1
36.70	1	28.40	1
30.20	1	34.30	1
36.50	1	27.30	1
33.00	1	27.90	1
34.70	1	28.50	1
29.00	1	28.50	1
36.60	1	29.10	1
35.70	1	33.10	1
36.20	1	33.00	1
33.20	1	30.10	1
36.00	1	33.10	1
37.20	1	33.40	1
37.20	1	29.00	1
35.60	1	31.00	1
27.30	1	36.40	1
32.80	1	35.70	1
32.20	1	29.90	1
33.40	1	35.30	1
34.70	1	32.60	1
29.60	1	35.90	1
33.60	1	35.00	1
34.00	1	35.70	1
27.09	1	31.20	1
32.20	1	33.10	1
Average = 33.10		Average = 31.95	

Failure Mode : 1 – Shear with Ball Lifted

Sample 8/9 : Copper chip (plated with silver) mounted on BGA substrate using QMI518

Curing profile : 150 degrees Celsius for 1hr.

Bonding equipment: ESEC 3018 Wire Bonder

Hight Temp. Storage (at 150 deg C for 1 Hr) Before Gold Ball Bonding		Hight Temp. Storage (at 150 deg C for 1 Hr) Before Wedge Bonding	
Pull Strength (grams)	Failure Mode	Pull Strength (grams)	Failure Mode
9.922	1	7.924	1
10.285	1	7.518	1
9.962	1	8.512	1
10.510	1	8.087	1
10.470	1	8.428	1
10.059	1	8.041	1
10.541	1	8.605	1
10.169	1	8.265	1
9.980	1	8.361	1
10.303	1	8.309	1
10.450	1	7.797	1
10.439	1	7.464	1
9.578	1	8.430	1
9.667	1	8.291	1
9.734	1	8.004	1
9.768	1	8.162	1
9.580	1	8.110	1
9.176	1	8.428	1
10.112	1	8.152	1
9.896	1	8.391	1
10.583	1	7.353	1
9.920	1	7.897	1
9.410	1	7.774	1
10.055	1	7.816	1
9.991	1	8.128	1
10.763	1	8.248	1
10.806	1	8.240	1
10.938	1	8.537	1
10.358	1	8.204	1
10.965	1	8.159	1
Average = 10.146		Average = 8.121	

Failure Mode : 1 – Break at the Ball Neck (for gold bond)

1 - Break at the 1st bond Heel (for wedge bond)

APPENDIX – B